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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,765	01/09/2002	David P. Sonnier	LUCT-123744B	8338

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EXAMINER	
MATTIS, JASON E	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/21/2007.

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docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/044,765	SONNIER, DAVID P.	
	Examiner	Art Unit	
	Jason E. Mattis	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination filed 11/28/06. Claims 1-20 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. (U.S. Publication US 2002/0085578 A1) in view of Lo et al. (U.S. Pat. 6667983 B1) and Lee (U.S. Pat. US 6963576 B1).

With respect to claims 1 and 8, Dell et al. discloses a method in a network system that employs packets having an associated priority **(See the abstract and page 8 paragraph 106 for reference to a network switch, which is a network system, that employs packets having an associated priority)**. Dell et al. also discloses at least two inputs configured to receive packets and at least three packet first-in-first-out buffers (FIFOs) configured to receive packets from the inputs **(See page 3 paragraphs 48-49, page 8 paragraph 107, and Figures 2 and 10 of Dell et al. for reference to**

crossbar device 206 having inputs connecting to ingress line cards 202 and for reference to a number of routing FIFO queues, which are FIFO buffers configured to receive cells, which are data packets, from the inputs). Although Dell et al. does disclose the use of packet priority to cause a packet to be queued from one of the FIFOs for processing **(See page 8 paragraph 107 and page 10 paragraphs 145-153 of Dell et al. for reference to an arbiter selecting which bit to accept for the transfer and processing of a packet to an output FIFO queue and for reference to selecting based on a packet priority)**, Dell et al. does not specifically disclose a priority summarizer configured to generate a priority summary of the packets within the inputs and packet FIFOS and a scheduler configured to cause one of the packet FIFOs to be queued for processing based on the priority summary. Dell et al. also does not specifically disclose the packet FIFOs configured as subsets of packet FIFOs with each of the FIFOs in each of the subsets being coupled to a different one of the inputs.

With respect to claim 15, Dell et al. discloses a crossbar switch that employs packets having an associated **priority (See the abstract and page 8 paragraph 106 for reference to a network switch that employs packets having an associated priority)**. Dell et al. also disclose at least two physical interfaces with corresponding inputs and outputs and at least two packet first-in-first-out buffers (FIFOs) receiving packets from inputs **(See page 3 paragraphs 48-49, page 8 paragraph 107, and Figures 2 and 10 of Dell et al. for reference to crossbar device 206 having inputs and physical interfaces connecting to ingress line cards 202 and outputs connecting to egress line cards 210, for reference to each of the outputs having a**

number of corresponding routing FIFO queues, which are packet FIFOs, and for reference to each output also having a corresponding FIFO queue, which is a destination FIFO buffer, interposing the routing FIFOs and the outputs). Although Dell et al. does disclose the use of packet priority to cause a packet to be queued from one of the FIFOs for processing **(See page 8 paragraph 107 and page 10 paragraphs 145-153 of Dell et al. for reference to an arbiter selecting which bit to accept for the transfer and processing of a packet to an output FIFO queue and for reference to selecting based on a packet priority)**, Dell et al. does not specifically disclose a priority summarizer configured to generate a priority summary of the packets within the inputs and packet FIFOS and a scheduler configured to cause one of the packet FIFOs to be queued for processing based on the priority summary. Dell et al. also does not specifically disclose the packet FIFOs configured as subsets of packet FIFOs with each of the FIFOs in each of the subsets being coupled to a different one of the inputs.

With respect to claims 2, 9, and 16, Dell et al. does not disclose that the summary indicates which FIFO contains a packet having the highest priority.

With respect to claims 3, 10, and 17, Dell et al. does not disclose that the summary indicates an order in which to transmit packets contained in the FIFOs to a destination FIFO based upon packet priority.

With respect to claims 5, 12, and 19, Dell et al. does not disclose the summarizer generating a summary of packets within each of the packet FIFOs and within each source FIFO.

With respect to claims 1-3, 5, 8-10, 12, 15-17, and 19, Lo et al., in the field of communications, disclose a priority summarizer configured to generate a priority summary of the packets within the inputs and packet FIFOS indicating the FIFO with the highest priority packet **(See column 9 line 10 to column 10 line 41 and Figure 7 of Lo et al. for reference to circuit 405, which is a priority summarizer, storing lists of pointers to packets that are waiting in FIFOs to be transmitted with the lists of pointers being organized according to packet priority for each FIFO such that the lists are a priority summary of all packets within the FIFOs with the highest priority list being the list containing the packet with the highest priority)**. Lo et al. also discloses a scheduler configured to cause one of the packet FIFOs to be queued for processing based on an order indicated by the priority summary **(See column 10 line 42 to column 11 line 44 and Figures 8A-B of Lo et al. for reference to arbiter circuit 420, which is a scheduler, that selects a FIFO to be processed for packet transmission based on the priority information of packets stored in the FIFOs of circuit 405)**. Using a priority summarizer and a scheduler has the advantage of allowing all packets to be fairly serviced while giving transmission priority to some packets over other packets regardless of the order in which the packets were received.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Lo et al., to combine the priority summarizer and scheduler, as disclosed by Lo et al., with the system and method of Dell et al., with the motivation being to allow all packets to be fairly serviced while giving transmission

priority to some packets over other packets regardless of the order in which the packets were received.

With respect to claims 1, 8, and 15, Lee, in the field of communications, discloses packet FIFOs configured as subsets of packet FIFOs with each of the FIFOs in each of the subsets being coupled to a different input **(See column 2 line 61 to column 3 line 31 and Figure 2 of Lee for reference to grouping virtual output queues in sets with each output port having a different corresponding arbiter 20 that arbitrates among a set of queues with each queue in the set of queues corresponding to a different input, i.e. arbiter 20A for output port 1 arbitrates among a set of virtual queues consisting of VOQ(1,1), VOQ(2,1), VOQ(3,1), and VOQ(4,1) corresponding to different input ports 1, 2, 3, and 4 respectively)**. Using packet FIFOs configured as subsets of packet FIFOs with each of the FIFOs in each of the subsets being coupled to a different input has the advantage of preventing head-of-line blocking **(See column 3 lines 20-31 for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Krishna et al., to combine using packet FIFOs configured as subsets of packet FIFOs with each of the FIFOs in each of the subsets being coupled to a different input, as suggested by Lee, with the system and method of Dell et al. and Lo et al., with the motivation being to prevent head-of-line blocking.

With respect to claims 4, 11, and 18, Dell et al. discloses that each of the inputs includes a source FIFO **(See page 3 paragraph 49 and Figure 2 of Dell et al. for reference to the inputs having queues, which are source FIFOs)**.

With respect to claims 6, 13, and 20, Dell et al. disclose a destination FIFO and an output with the destination FIFO interposing the packet FIFOs and the output **(See page 3 paragraphs 48-49, page 8 paragraph 107, and Figures 2 and 10 of Dell et al. for reference to crossbar device 206 having outputs connecting to egress line cards 210 and for reference to each output having a corresponding FIFO queue, which is a destination FIFO, interposing the routing FIFOs and the outputs)**. Dell et al. also discloses a scheduler transferring packets from the packet FIFOs toward the destination FIFO for transmission via the output **(See pages 8-9, paragraphs 111-120, pages 9-10 paragraphs 128-137, and Figures 12 and 15-16 of Dell et al. for reference to grants being accepted to transmit packets to FIFOs corresponding to outputs such that the packets are then outputted)**.

With respect to claims 7 and 14, Dell et al. disclose assigning the packet priority based on a priority associated with each of the inputs or a destination **(See page 10 paragraphs 145-153 for reference to selecting packets to transfer both from inputs and toward outputs based on priorities of the inputs an outputs)**.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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